This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) The expansion circuit according to claim 32,

wherein said internal signal is ~~logic circuit generates~~ an internal strobe signal ~~in response to said direct transition between said first state and said second state of said first and second signals~~;

further comprising a register with a clock signal coupled to said internal strobe signal and with one or more input lines coupled to one or more data signals from said host controller;

wherein said host controller is configured to ~~generate said direct transition from said first state to said second state to~~ perform output to said register.

2. (Previously Presented) The expansion circuit according to Claim 1 wherein said logic circuit comprises the logical equivalent of a three-input AND gate coupled to said first and second signals and a delay element coupled to said second signal and to said three-input AND gate, wherein said internal strobe is coupled to the output of said three-input AND gate.

3. (Previously Presented) The expansion circuit according to Claim 1 wherein said logic circuit comprises the logical equivalent of a three-input AND gate coupled to said first and second signals, a delay element coupled to said second signal and to said three-input AND gate, a two-input AND gate coupled to said first signal, and a two-input OR gate coupled to said three-input AND gate and to said two-input AND gate, wherein the output of said two-input OR gate is coupled to said two-input AND gate and wherein said internal strobe is coupled to the output of said two-input OR gate.

4. (Previously Presented) The expansion circuit according to Claim 1 wherein:

said first state consists of the state when said first signal is at a logic low level and said second signal is at a logic low level; and

said second state consists of the state when said first signal is at a logic low level and said second signal is at a logic high level.

5. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform input from or output to said peripheral device ~~to prevent said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal to a logic high state;

(b) setting said second signal to said second new state; and

(c) setting said first signal to said first new state.

6. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform input from or output to said peripheral device ~~to prevent said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;

(b) if said second previous state is not the same as said second new state, setting said second signal to said second new state; and

(c) if said first new state is not a logic high, setting said first signal to said first new state.

7. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform output to said register ~~to generate said direct transition from said first state to said~~

~~second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal to a logic high state;

(b) setting said second signal to a logic low state;

(c) setting said first signal to a logic low state;

(d) setting said second signal to a logic high state;

(e) setting said first signal to a logic high state;

(f) setting said second signal to said second new state; and

(g) setting said first signal to said first new state.

8. (Previously Presented) The expansion circuit according to Claim 7 further comprising the step of setting said data signals to a state consisting of desired output data before said step (d).

9. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform output to said register ~~to generate said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;

(b) if said second previous state is not a logic low state, setting said second signal to a logic low state;

(c) setting said first signal to a logic low state;

(d) setting said second signal to a logic high state;

(e) setting said first signal to a logic high state;

(f) if said second new state is not a logic high state, setting said second signal to said second new state; and

(g) if said first new state is not a logic high state, setting said first signal to said first new state.

10. (Previously Presented) The expansion circuit according to Claim 9 further comprising the step of setting said data signals to a state consisting of desired output data before said step (d).

11. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform output to said register ~~to generate said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal and said second signal to a logic low state;

(b) setting said second signal to a logic high state;

(c) setting said first signal to a logic high state; and

(d) setting said first signal and said second signal to said first new state and said second new state respectively.

12. (Previously Presented) The expansion circuit according to Claim 11 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

13. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform output to said register ~~to generate said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first

signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic low state, setting said first signal to a logic low state, and if said second previous state is not a logic low state, setting said second signal to a logic low state;

(b) setting said second signal to a logic high state;

(c) setting said first signal to a logic high state; and

(d) if said first new state is not a logic high state, setting said first signal to said first new state, and if said second new state is not a logic high state, setting said second signal to said second new state.

14. (Previously Presented) The expansion circuit according to Claim 13 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

15. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform output to said register ~~to generate said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal and said second signals to a logic low state;

(b) setting said second signal to a logic high state; and

(c) setting said first signal and said second signal to said first new state and said second new state respectively.

16. (Previously Presented) The expansion circuit according to Claim 15 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

17. (Currently Amended) The expansion circuit according to Claim 4 wherein to perform output to said register ~~to generate said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic low state, setting said first signal to a logic low state, and if said second previous state is not a logic low state, setting said second signal to a logic low state;

(b) setting said second signal to a logic high state; and

(c) if said first new state is not a logic low state, setting said first signal to said first new state, and if said second new state is not a logic high state, setting said second signal to said second new state.

18. (Previously Presented) The expansion circuit according to Claim 17 further comprising the step of setting said data signals to a state consisting of desired output data before said step (b).

19. (Withdrawn – Currently Amended) The expansion circuit of claim 32:

wherein said internal signal is ~~logic circuit activates~~ an internal enable signal ~~in response to said direct transition between said first state and said second state of said first and second signals, and deactivates said internal enable signal in response to a transition between said second state and a third state of said first and second signals~~;

further comprising a buffer with enable line coupled to said internal enable signal and with one or more output lines coupled to one or more data lines of said host controller;

wherein said host controller is configured to ~~generate said direct transition from said first state to said second state, and to generate said transition from said second state to said third state to~~ perform input from said buffer.

20. (Withdrawn) The expansion circuit according to Claim 19 wherein said logic circuit comprises the logical equivalent of a three-input AND gate coupled to said first and second signals, a delay element coupled to said second signal and to said three-input AND gate, a two-input AND gate coupled to said first signal, and a two-input OR gate coupled to said three-input AND gate and to said two-input AND gate, wherein the output of said two-input OR gate is coupled to said two-input AND gate and wherein said internal enable is coupled to the output of said two-input OR gate.

21. (Withdrawn – Currently Amended) The expansion circuit according to Claim 19 wherein:

said first state consists of the state when said first signal is at a logic low level and said second signal is at a logic low level;

said second state consists of the state when said first signal is at a logic low level and said second signal is at a logic high level~~; and said third state consists of the state when said first signal is at a logic high level and said second signal is at a logic high level~~.

22. (Withdrawn – Currently Amended) The expansion circuit according to Claim 21 wherein to perform input from or output to said peripheral device ~~to prevent said direct transition from said first state to said second state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal to a logic high state;

(b) setting said second signal to said second new state; and

(c) setting said first signal to said first new state.

23. (Withdrawn – Currently Amended) The expansion circuit according to Claim 21 wherein to perform input from or output to said peripheral device ~~to prevent said direct transition from said first state to said second state~~, said host controller is configured to

change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;

(b) if said second previous state is not the same as said second new state, setting said second signal to said second new state; and

(c) if said first new state is not a logic high, setting said first signal to said first new state.

24. (Withdrawn – Currently Amended) The expansion circuit according to Claim 21 wherein to perform input from said buffer ~~to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal to a logic high state;

(b) setting said second signal to a logic low state;

(c) setting said first signal to a logic low state;

(d) setting said second signal to a logic high state;

(e) setting said first signal to a logic high state;

(f) setting said second signal to said second new state; and

(g) setting said first signal to said first new state.

25. (Withdrawn) The expansion circuit according to Claim 24 further comprising the step of reading the state of said data signals between step (d) and step (e).

26. (Withdrawn – Currently Amended) The expansion circuit according to Claim 21 wherein to perform input from said buffer ~~to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic high state, setting said first signal to a logic high state;

(b) if said second previous state is not a logic low state, setting said second signal to a logic low state;

(c) setting said first signal to a logic low state;

(d) setting said second signal to a logic high state;

(e) setting said first signal to a logic high state;

(f) if said second new state is not a logic high state, setting said second signal to said second new state; and

(g) if said first new state is not a logic high state, setting said first signal to said first new state.

27. (Withdrawn) The expansion circuit according to Claim 26 further comprising the step of reading the state of said data signals between step (d) and step (e).

28. (Withdrawn – Currently Amended) The expansion circuit according to Claim 21 wherein to perform input from said buffer ~~to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) setting said first signal and said second signal to a logic low state;

(b) setting said second signal to a logic high state;

(c) setting said first signal to a logic high state; and

(d) setting said first signal and said second signal to said first new state and said second new state respectively.

29. (Withdrawn) The expansion circuit according to Claim 28 further comprising the step of reading the state of said data signals between step (b) and step (c).

30. (Withdrawn – Currently Amended) The expansion circuit according to Claim 21 wherein to perform input from said buffer ~~to generate said direct transition from said first state to said second state and to generate said direct transition from said second state to said third state~~, said host controller is configured to change ~~changes~~ the state of said first signal from a first previous state to a first new state and said second signal from a second previous state to a second new state by performing the steps of:

(a) if said first previous state is not a logic low state, setting said first signal to a logic low state, and if said second previous state is not a logic low state, setting said second signal to a logic low state;

(b) setting said second signal to a logic high state;

(c) setting said first signal to a logic high state; and

(d) if said first new state is not a logic high state, setting said first signal to said first new state, and if said second new state is not a logic high state, setting said second signal to said second new state.

31. (Withdrawn) The expansion circuit according to Claim 30 further comprising the step of reading the state of said data signals between step (b) and step (c)

32. (Currently Amended) An expansion circuit for an embedded system comprising a host controller and a peripheral device, said expansion circuit comprising:

a logic circuit coupled to first and second signals, said first and second signals coupled to said host controller and to said peripheral device, said logic circuit generating an internal signal in response to the condition wherein said first and second signals transition directly between a first state and a second state ~~a direct transition between a first state and a second state of said first and second signals~~;

wherein said host controller is configured such that said first and second signals transition to a third state after said first state and before said second state ~~to prevent a direct transition from said first state to said second state~~ when ~~changing~~ the state of said first and second signals are changed as necessary to perform input from ~~to~~ or output to ~~from~~ said peripheral device; and

wherein said host controller is configured such that said first and second signals transition directly between said first state and said second state ~~to generate a direct transition from said first state to said second state~~ when the state of said first and second signals are changed as necessary to perform input from or output to said expansion circuit ~~to generate said internal signal~~.